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09/501,045	02/09/2000	Glenn T. Colon-Bonet	10971158-1	3338

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/501,045	COLON-BONET, GLENN T.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8,10,23-35 and 37-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8,10,23-35 and 37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/18/2006.

2. Claims 1-2, 7-8, 10, 23-35, and 37-40 are pending in this application. Claims 1, 7, and 35 are independent claims. In Amendment, claims 3-6, 9, 11-22, and 36 are cancelled and claim 40 is added. This Office Action is made non-final after a RCE filed 08/18/2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 7-8, 23-25, 27-30, 32-35, and 37-40 are rejected under 35 U.S.C. 103(a) as being obvious over Knowles (U.S. 6,446,107) in view of Taewhan et al. ("Arithmetic Optimization using Carry-Save-Adders").

Re claim 1, Knowles discloses in Figure 3 an apparatus (e.g. abstract and col. 9 line 59 – col. 10 line 10) for performing addition of propagate, kill, and generate recoded numbers (e.g. each pair of bits in Figure 3 are encoded as PKG for OR, AND, and XOR logic gate respectively), apparatus comprising: circuitry (e.g. circuitry in Figure 3, for now the top portion of Figure 3 will be used for illustrating) configured to receive at least a first operand (e.g. PKG of a0 and b0), a second operand (e.g. PKG of a1 and b1), and a

carry-in bit (e.g. Co input goes into dash-line box 26), the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands (e.g. output of 6_0 as kill, output of 2_0 as generate, output of XOR as propagate; similarly for a1 and b1); a first adder (e.g. a mid portion of Figure 3 including 8_0, 10_0, 8_1 logic gate and attached XOR gate which interfaces with all p, k, and g of a0-a1 and b0-b1) configured to add first operand (e.g. representations of a0 and b0) and second operand (e.g. representation of a1 and b1) to generate a third propagate, kill, and generate recoded number representation (e.g. outputs go to 24_0 and 24_1 logic gates) and a carry-out bit (e.g. output of second level OR next to 8_1 AND gate which carry to the next bit); and a modified adder (e.g. last portion of Figure 3 including 24_0, and 24_1) configured to receive the third propagate, kill, and generate recoded number representation from the first adder (e.g. all inputs go to 24_0 and 24_1 logic gates), and the carry-in bit from the circuitry (e.g. C_0 goes into 24_0 logic gate), add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value (e.g. S0, S0' by the first XOR logic gate 24_0) and a carry value (e.g. output of 10_0 to the next bit or S1,S1') wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output (e.g. output of OR gate attached to 8_1 logic gate) and the carry value from the modified adder at a second output (e.g. Figure 3), wherein each of the propagates, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits (e.g. col. 9 line 59 – col. 10 line 10),

wherein the kill bit, if set (e.g. col. 10 lines 17-21 as bar(k_i)), indicates that each of the bits of the respective coded logical value is not sets wherein the propagate bit, if set (e.g. p = a exor b in line 65 col. 9 wherein the propagate bit goes high or 1 only if either a or b is high or col. 10 lines 15-17), indicates that only one of the bits of the respective coded logical value is sets and wherein the generate bit, if set (e.g. g = a*b in line 64 col. 9 wherein the generate bit goes high or 1 only if both a and b are high or col. 10 lines 12-14), indicates that two of the bits of the respective coded logical value are set. Knowles fails to disclose the first and modified adder is the carry-save adder. However, Taewhan et al. disclose the carry-save adder is the most often used type in implementing a fast computation of arithmetic in industry (e.g. abstract). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the carry-save adder as seen in Taewhan et al.'s invention into the first and modified adder in Knowles' invention because it would enable to compute addition faster in hardware implementation (e.g. abstract and first paragraph under introduction section).

Re claim 7, it is a method claim of claim 1. Thus, claim 7 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 8, Knowles further discloses in Figure 3 logically combining comprises adding the third propagate, kill, and generate representation and the carry-in value (e.g. 24_0, and 24_1 logic gates).

Re claim 23, Knowles further discloses in Figure 3 the sum value is a function of the third propagate representation and the carry-in value (e.g. 24_0 wherein it takes the value of C_0 as carry-in and output of EXOR gate as the third propagate representation).

Re claim 24, Knowles further discloses in Figure 3 the sum value is the XOR combination of the third propagate representation and the carry-in value (e.g. 24_0 is the XOR logic gate).

Re claim 25, Knowles further discloses in Figure 3 the carry value is a function of the third propagate representation, the carry-in value, and the third generate representation (e.g. 24_1 including output of XOR gate 10_0 and output of XOR gate).

Re claim 27, Knowles further discloses in Figure 3 the carry-out value is a function of the first and second generate representations (e.g. output of OR gate adjacent to 8_1).

Re claim 28, Knowles further discloses in Figure 3 the carry-out value is the OR combination of the first and second generate representations (e.g. output of OR gate adjacent to 8_1 indirectly).

Re claim 29, Knowles further discloses in Figure 3 the circuitry provides the sum value at a third output (e.g. 24_0).

Re claim 30, Knowles further discloses in Figure 3 logically combining comprises a XOR combination of the third propagate representation and the carry-in value (e.g. 24_0).

Re claim 32, Knowles further discloses in Figure 3 step of generating comprises an OR combination of the first and second generate representations (e.g. output of OR gate adjacent to 8_1 indirectly).

Re claim 33, Knowles further discloses in Figure 3 only one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number

representation can simultaneously be at the particular binary value (e.g. col. 9 line59 – col. 10 line 10).

Re claim 34, Knowles further discloses in Figure 3 each set bit of the logical value has a binary value of one (e.g. col. 10 lines 11-21).

Re claim 35, Knowles discloses in Figure 3 apparatus (e.g. abstract and col. 9 line 59 – col. 10 line 10) for performing addition, apparatus comprising: a first carry save adder (e.g. circuitry in Figure 3, for now the top portion of Figure 3 will be used for illustration) configured to receive a first operand defining a first logical value encoded in propagate, kill, and generate (PKG) form such that the operand has a propagate bit, a generate bit, and a kill bit (e.g. PKG of a0 and b0…), the first carry save adder (e.g. circuitry in Figure 3, for now the top portion of Figure 3 will be used for illustration) configured to receive a second operand defining a second logical value encoded in PKG form (e.g. PKG of a0/1 and b0/1…) such that the second operand has a propagate bit, a generate bit, and a kill bit (e.g. PGK respectively), the first carry save adder (e.g. circuitry in Figure 3, for now the top portion of Figure 3 will be used for illustration) further reconfigured to sum the first and second operands in PKG form to provide a first sum output in PKG form and a first carry bit (e.g. outputs go to 24_0 and 24_1 logic gates and output of second level OR next to 8_1 AND gate which carry to the next bit respectively) without decoding the first and second operands from PKG form (e.g. Figure 3), the first sum output having a propagate bit, a generate bit, and a kill bit, wherein the first carry bit and the propagate, generate, and kill bits of the first sum output collectively represent a summation of the first second operands (e.g. as input into the second logical adder with

last portion of Figure 3 including 24_0 and 24_1) wherein the first sum output represents a third logical value encoded in PKG form, wherein the third logical value has a plurality of bits (e.g. col. 9 line 59 – col. 10 line 10), wherein the kill bit, if at a particular binary value (e.g. col. 10 lines 17-21), indicates that none of the bits of the logical value are set, wherein the propagate bit, if at the particular binary value (e.g. p = a exor b in line 65 col. 9 wherein the propagate bit goes high or 1 only if either a or b is high or col. 10 lines 15-17), indicates that only one of the bits of the logical value is set, and wherein the generate bit, if at the particular binary value (e.g. g = a*b in line 64 col. 9 wherein the generate bit goes high or 1 only if both a and b are high or col. 10 lines 12-14), indicates that two bits of the logical value are set. Knowles fails to disclose the adder is the carry-save adder. However, Taewhan et al. disclose the carry-save adder is the most often used type in implementing a fast computation of arithmetic in industry (e.g. abstract). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the carry-save adder as seen in Taewhan et al.'s invention into the adder in Knowles' invention because it would enable to compute addition faster in hardware implementation (e.g. abstract and first paragraph under introduction section).

Re claim 37, it is a method claim of claim 34. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 34.

Re claim 38, Knowles further discloses in Figure 3 on a respective one of the kill, propagate, and generate bit of each possible propagate, kill, and generate recorded number representation can be set (e.g. p, g, and bar(k)).

Re claim 39, it has same limitation as cited in claim 38. Thus, claim 39 is also rejected under the same rationale as cited in the rejection of rejected claim 38.

Re claim 40, Knowles further discloses in Figure 3 a second carry save adder (e.g. last portion of Figure 3 including 24_0 and 24_1) configured to receive a second carry bit and the first sum output of the first carry save adder, the second carry save adder (e.g. last portion of Figure 3 including 24_0 and 24_1) configured to sum the first sum output and the second carry bit to provide a second sum output having a carry bit and a sum bit.

5. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Knowles (U.S. 6,446,107) in view of Taewhan et al. ("Arithmetic Optimization using Carry-Save-Adders"), as applied to claims 1 and 7 respectively above, and further in view of Miller (U.S. 5,706,323).

Re claim 2, Knowles in view of Taewhan et al. do not disclose sum value and carry value are dual rail encoded values. However, Miller discloses a method of encoding variables into dual rail values in Figure 3. Therefore, it would have been obvious to a person having ordinary skill in the art to encode the sum value and carry value as dual rail values as seen in Miller's invention into Knowles in view of Taewhan et al.s' invention because it would simplify the circuitry and reduce the noise.

Re claim 10, it is a method claim of claim 2. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Allowable Subject Matter

6. Claims 26 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed 08/18/2006 have been fully considered but they are not persuasive.

a. The applicant argues in pages 10-12 for claim 1 and similarly argument for claim 7 in pages 13-14 that the cited reference fails to disclose the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set as seen in the claimed invention because the labeled "bar(K_1)" cannot be same as the kill stated in the claim, particularly bar(K_1) in the reference is just an OR of a_i and b_i which is not same as claimed.

The examiner respectfully submits that the cited reference has addressed in detail the kill bit as required in the claim invention. Generally, the applicant had agreed with the examiner the table listed in page 11 of the remark that the bar(kill), if set, indicates that each of the bits of the respective coded logical value is not set. Since the claim does not define the particular logic gate structure of the kill bit, but rather the claim only defines the logical value of the kill bit. Thus, any bit, regardless how it is called, would be the kill bit if it meets the definition of the kill bit which is defined in the claim. Again, the kill bit of the claimed invention is

the bar(kill) bit of the cited reference because the bar(kill) of the cited reference clearly meets the required definition of the kill bit of the claimed invention. As clearly seen in columns 9-10 of the cited reference and mathematically the kill bit as $k_i = a_i+b_i$ and the $bar(k_i) = bar(a_i+b_i) = bar(a_i)*bar(b_i)$. In addition, the invention of the cited reference only utilizes the bar(k) as seen in equations 4-5 of Figures 9B and 9C. Thus, the $bar(k_i)$ (e.g. same as kill bit in the application) is only set if a_i and b_i are not set due to expression above which clearly meets the definition of the claimed invention.

b. The applicant argues in pages 12-13 for claim 33 that the cited reference fails to disclose the limitation of only a respective one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can be set.

The examiner respectfully submits that in view of the above argument, the cited reference clearly discloses the limitation of only a respective one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can be set which can be seen in the table addressed by examiner in pages 11-12 which also agreed by the applicant in page 12 first paragraph. From the table, bar(kill), G, and P is alternatively set at any moment.

c. The applicant argues in pages 15-16 for claim 35 that the cited reference fails to disclose the first carry save adder further configured to sum the first and second operands in PKG form to provide a first sum output in PKG form and a first carry bit without

decoding the first and second operands form PKG form, the first sum output having a propagate bit, a generate bit, and a kill bit.

The examiner respectfully submits that claim 35 does not define clearly individual definition of each of PKG bits wherein the output PKG bits of the first carry-save adder is not the same as input PKG bits of the first carry-save adder as seen in Figure 5 of claimed invention. Thus, as long as there are three output bits from the first carry-save adder, they can be considered as output PKG bits of the first carry-save adder. Therefore, Figure 3 of the cited reference clearly addresses the limitations above wherein the first carry-save adder is logic gates 8_0, 10_0, and OR gate (e.g. middle portion of Figure 3) which receives the first and second operands in PKG form (e.g. first operand PKG form is the output of OR, AND, and XOR gate of a_0 and b_0 and the second operand PKG form is the output of OR, AND, and XOR gate of a_1 and b_1) to provide the first sum output in PKG form (e.g. outputs of 1st XOR, OR as 10_0, and 2nd XOR as PKG form) and a first carry bit (e.g. output of 2nd OR gate) without decoding the first and second operands form PKG form (e.g. the operation is done directly without decoding back to a and b operand as seen in Figure 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

September 27, 2006